



RADIATED EMISSION

Model Name : CDS4004803

Model No. :

Serial No. :

Points : 2

Detector : PEAK/QP

Polarization : Hori. & Vert.

Tested by : J.Hatagishi

Temp. : 25degC

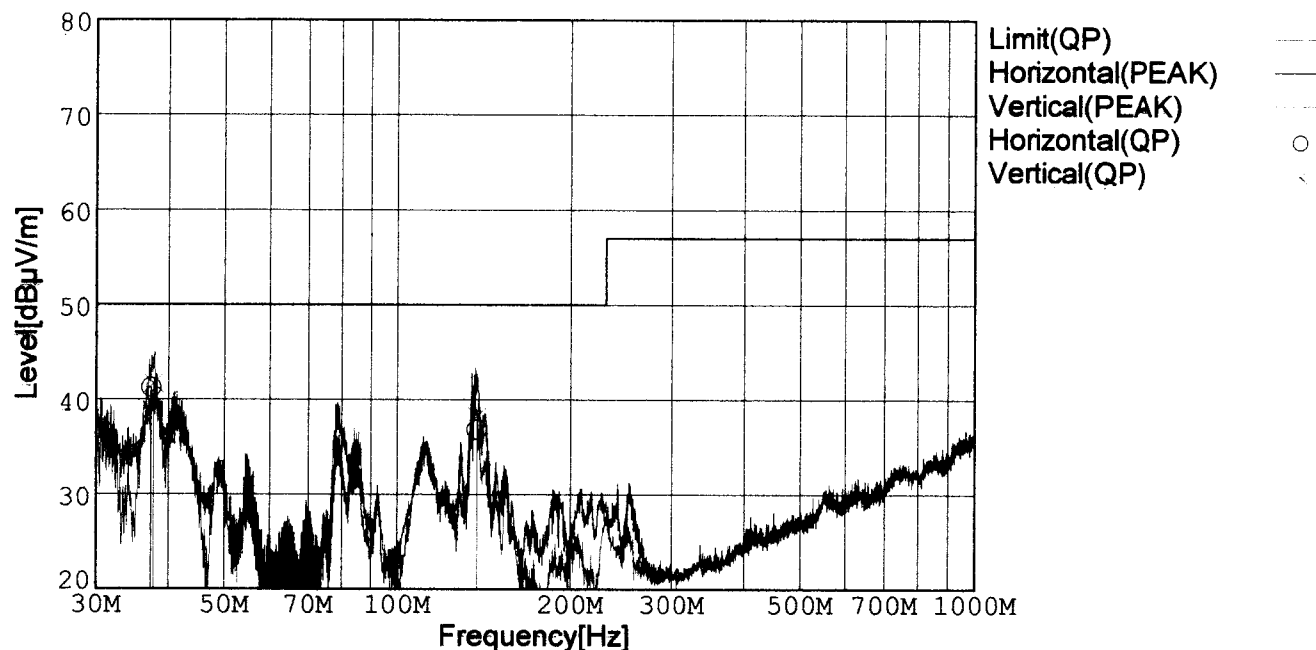
Humi. : 40%

Date : 2002/3/9 5:16

Test Equip. : R3132,ESPC

Comment : Vin=DC48V Io=100% (3.3V 100A)

Limit: [EN 55022] Class A<3m>



Frequency [MHz]	Meter Reading (QP) [dBμV]	Ant. Type	Antenna Factor [dB/m]	Cable & Preamp [dB]	Level (QP) [dBμV/m]	Angle[°]	Height [cm]	Polar.	Limit [dBμV/m]	Margin [dB]
37.377	48.3	BL	14.5	-21.6	41.2	240	109	Hori.	50.0	8.8
137.314	46.9	BL	10.9	-21.0	36.8	316	128	Hori.	50.0	13.2
37.748	49.1	BL	14.2	-21.6	41.7	187	101	Vert.	50.0	8.3
137.460	48.3	BL	10.9	-21.0	38.2	358	123	Vert.	50.0	11.8

BL: Biconi-Log

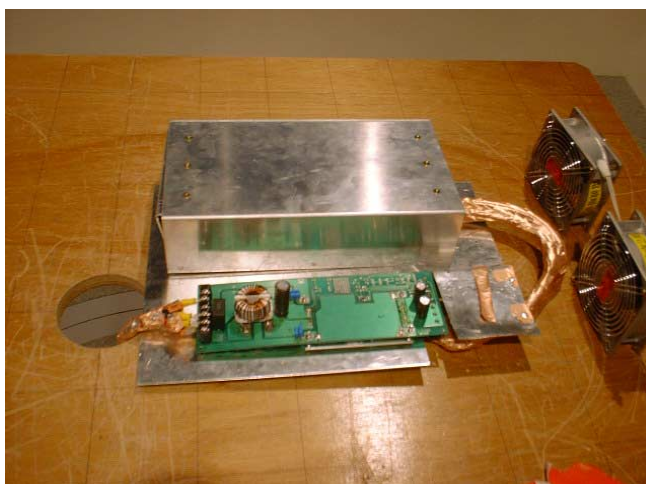
Conditions

Date 2002/3/9

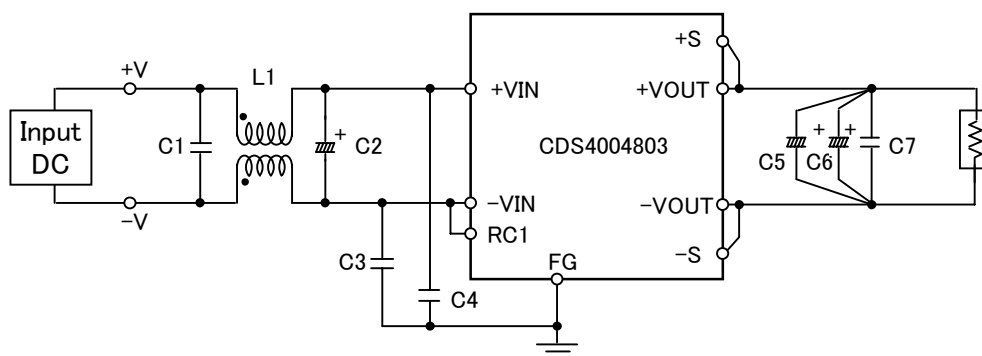
Test : RADIATED EMISSION

Model Name : CDS4004803

○Photographs of Test Set-Up



○Testing circuitry



L1	: 1mH	SC15-10JH (TOKIN)
C1	: 0.68 μ F	CFJC22E684M (NITSUKO)
C2	: 100V 470 μ F	PM series (NICHICON)
C3,C4	: 630V 0.033 μ F	MDS22J333K (NITSUKO)
C5,C6	: 10V 3300 μ F	PW series (NICHICON)
C7	: 50V 0.1 μ F	MDD21H104M (NITSUKO)

Fig. Testing circuitry



LINE CONDUCTION

Model Name : CDS4004803

Model No. :

Serial No. :

Points : 3

Detector : PEAK/QP/Ave.

Line Mode : VA/VB

Limit1: [EN 55022] Class A(QP)

Limit2: [EN 55022] Class A(Ave.)

Tested by : J.Hatagishi

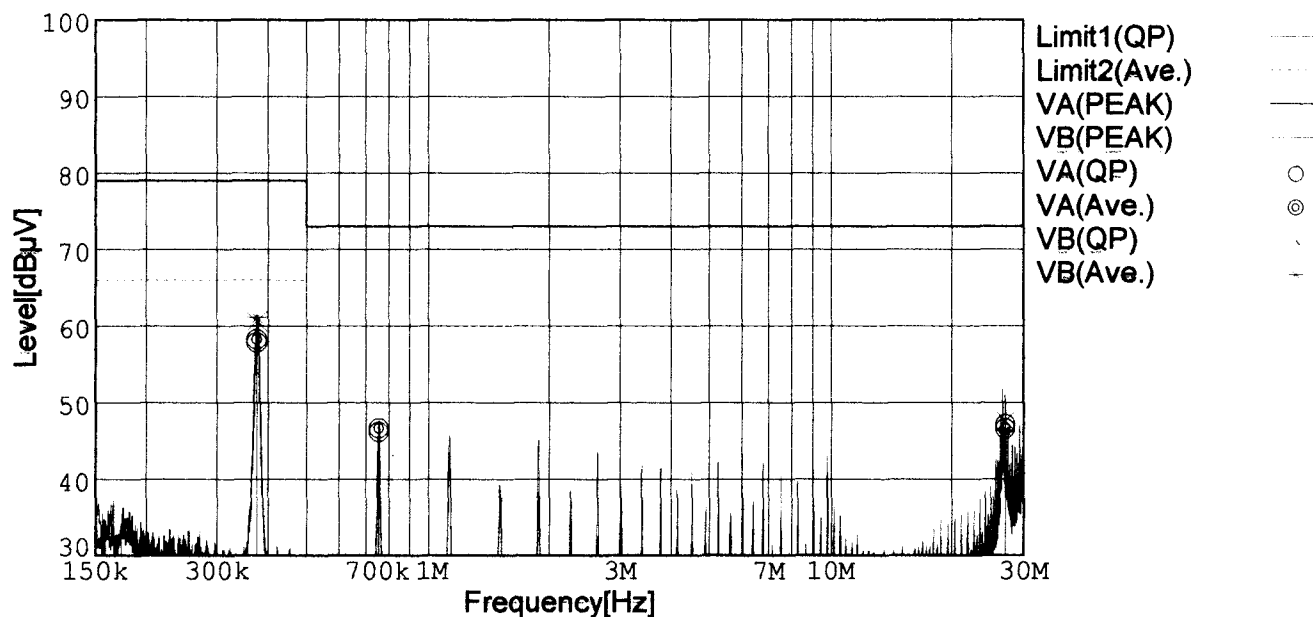
Temp. : 25degC

Humi. : 40%

Date : 2002/3/9 4:39

Test Equip. : R3132,ESPC

Comment : Vin=DC48V Io=100% (3.3V 100A)



Frequency [MHz]	Meter Reading (QP) [dBμV]	Meter Reading (Ave.) [dBμV]	Factor [dB]	Level (QP) [dBμV]	Level (Ave.) [dBμV]	Line	Limit (QP) [dBμV]	Limit (Ave.) [dBμV]	Margin (QP)[dB]	Margin (Ave.) [dB]
0.3755	48.0	48.4	9.8	57.8	58.2	VA	79.0	66.0	21.2	7.8
0.7528	36.2	36.7	9.9	46.1	46.6	VA	73.0	60.0	26.9	13.4
27.0761	36.7	36.1	10.4	47.1	46.5	VA	73.0	60.0	25.9	13.5
0.3757	50.8	51.3	9.8	60.6	61.1	VB	79.0	66.0	18.4	4.9
27.0709	37.1	36.0	10.4	47.5	46.4	VB	73.0	60.0	25.5	13.6

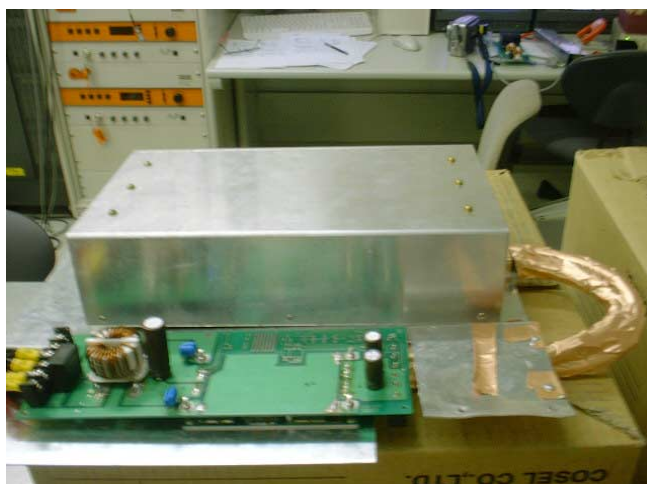
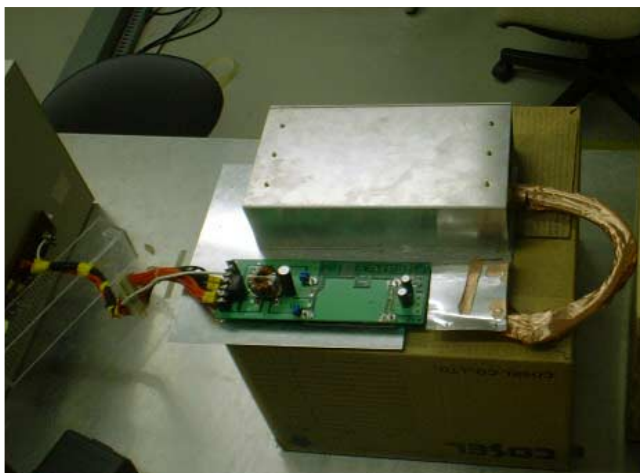
Conditions

Date 2002/3/9

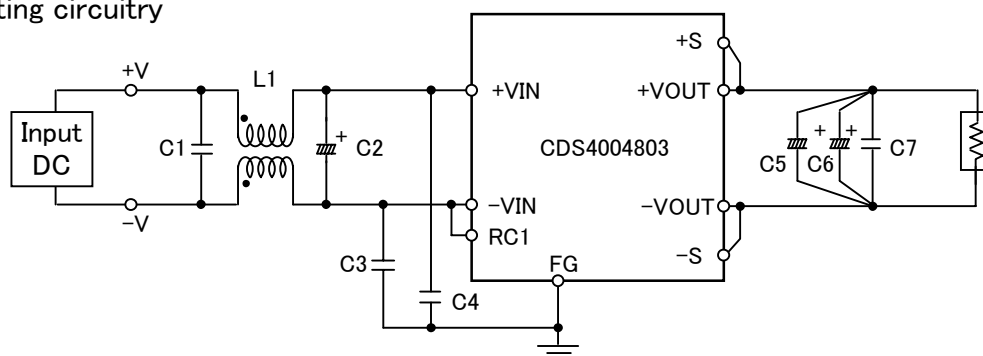
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○Photographs of Test Set-Up



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Fig. Testing circuitry