

SFS10/15/20 series EMI/EMS Test resultApproved : Toshiyuki Tsuru  
Toshiyuki TsuruPrepared : K. Shibutani  
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No.	Test item	Conditions	Conditions of Acceptability	Result
1	Line conduction	(1) Rated input (2) Rated load (3) Ambient temp. $25 \pm 10^{\circ}\text{C}$ (4) Testing circuitry Fig.1	(1) Meets the undermentioned standard. VCCI classA CISPR22 classA , EN55022-A	OK
2	Radiated emission	(1) Rated input (2) Rated load (3) Ambient temp. $25 \pm 10^{\circ}\text{C}$ (4) Testing circuitry Fig.1	(1) Meets the undermentioned standard. VCCI classA CISPR22 classA , EN55022-A	OK
3	Static electricity immunity test (EN61000-4-2)	(1) Rated input (2) Rated load (3) Ambient temp. $25 \pm 10^{\circ}\text{C}$ (4) Contact discharge voltage 8[kV] (EN61000-4-2 Level 4) (5) Testing circuitry Fig.2	(1) No protection circuit failure. (2) No output voltage drop with control circuit failure. (3) No any other function failure	OK
4	Radiated, radio-frequency, electromagnetic field immunity test (EN61000-4-3)	(1) Rated input (2) Rated load (3) Ambient temp. $25 \pm 10^{\circ}\text{C}$ (4) Testing field strength 10[V/m] (EN61000-4-3 Level 3) (5) Testing circuitry Fig.2	(1) No protection circuit failure. (2) No output voltage drop with control circuit failure. (3) No any other function failure	OK
5	Electrical fast transient/ burst immunity test (EN61000-4-4)	(1) Rated input (2) Rated load (3) Ambient temp. $25 \pm 10^{\circ}\text{C}$ (4) Test peak voltage 4[kV] (IEC61000-4-4 Level 4) (5) Testing circuitry Fig.2	(1) No protection circuit failure. (2) No output voltage drop with control circuit failure. (3) No any other function failure	OK
6	Surge immunity test (EN61000-4-5)	(1) Rated input (2) Rated load (3) Ambient temp. $25 \pm 10^{\circ}\text{C}$ (4) Test voltage Line to line 2[kV] (Level 3) (5) Testing circuitry Fig.3	(1) The power supply is not stop (2) Circuit does not malfunction. (3) No abnormality of the insulation destruction etc. (4) Parts are no damaged.	OK

## OEMI/EMS testing circuitry

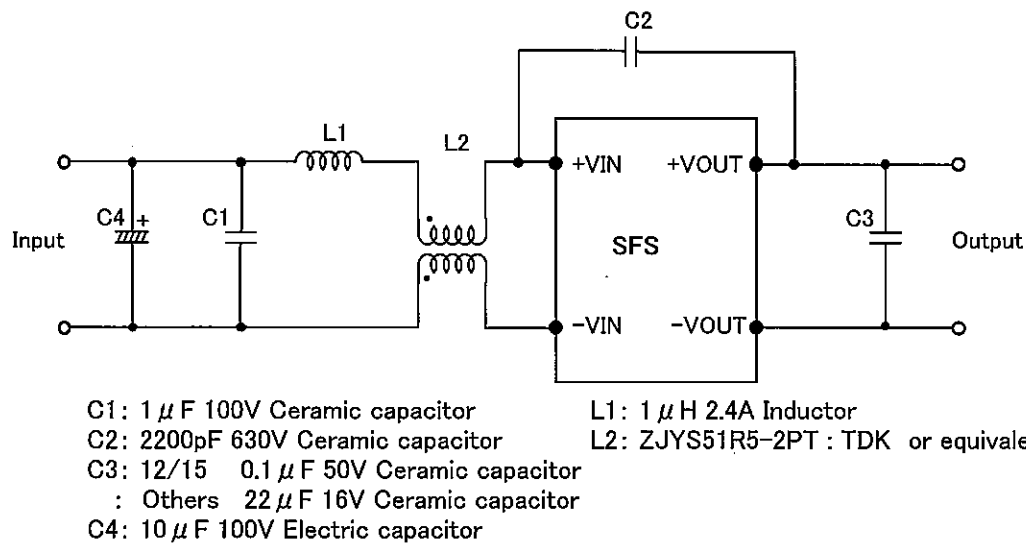


Fig.1 Testing circuitry (from No.1 and No.2)

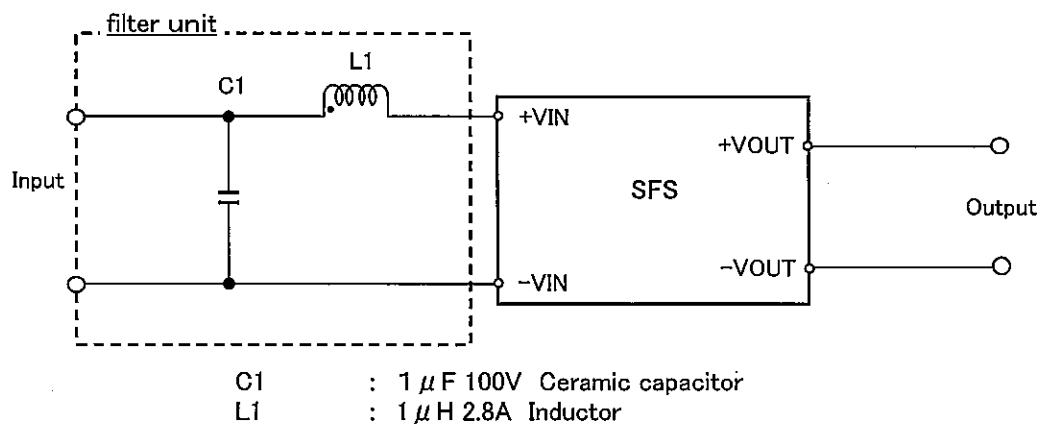


Fig.2 Testing circuitry (from No.3 to No.5)

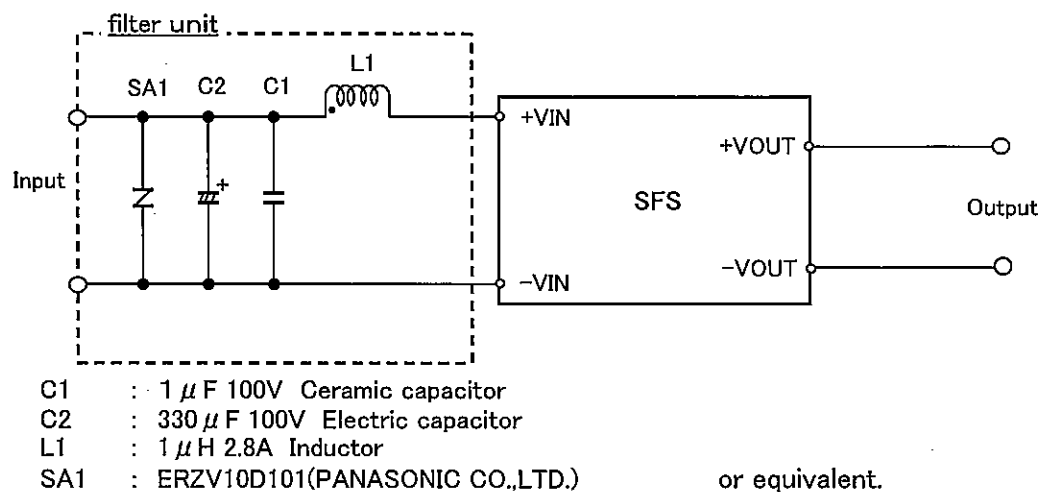


Fig.3 Testing circuitry (No.6)